What is claimed is:

1) A phase locked loop circuit, comprising:

a first circuit capable of providing a current representing frequency; and,

a second circuit, coupled to the first circuit, capable of providing a bias current responsive to the current.

2) The circuit of claim 1, wherein the current is obtained from a voltage regulator.

3) The circuit of claim 1, wherein the bias current is provided to a third circuit selected from the group consisting of a charge pump, a loop resistor, phase mixer, amplifier, clock buffer and an equivalent.

4) A delay locked loop circuit, comprising:

a first circuit capable of providing a current representing a delay; and,

a second circuit, coupled to the first circuit, capable of providing a bias current responsive to the current.

5) The circuit of claim 4, wherein the current is obtained from a voltage regulator.

6) The circuit of claim 5, wherein the bias current is provided to a third circuit selected from the group consisting of a charge pump, phase mixer, amplifier, clock buffer and an equivalent.

7) A phase locked loop circuit, comprising:

a phase-frequency detector capable of providing a phase difference signal responsive to an input signal and a feedback signal;

a first charge-pump, coupled to the phase-frequency detector, capable of providing a first voltage responsive to the phase difference signal;

a second charge pump, coupled to the phase-frequency detector, capable of providing a second voltage responsive to the phase difference signal;

a loop resistor, coupled to the first charge-pump, capable of providing a buffered voltage responsive to the first voltage,

a voltage regulator, coupled to the loop resistor and the second charge pump, capable of providing a current responsive to the buffered voltage and second voltage, wherein the voltage regulator includes a bias-generating device capable of providing a bias current;

a voltage-controlled oscillator, coupled to the voltage regulator, capable of providing the feedback signal responsive to the current; and,

an interconnect, coupled to the voltage regulator, the first charge pump, and the second charge pump, capable of providing the bias current.

8) The phase locked loop circuit of claim 7, wherein the bias-generating device in the voltage regulator is a MOSFET device.

9) The phase locked loop circuit of claim 8, wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and a source coupled a voltage source.

10) The phase locked loop circuit of claim 9, wherein the voltage regulator includes:

a second p-type transistor having a gate coupled to a gate of the first p-type transistor and a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the second transistor gate and a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the third transistor gate and a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the fourth transistor gate and a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, a source coupled to ground and a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain and the respective gates of the third and fourth p-type transistors, a gate coupled to an input, and a source;

a third n-type transistor having a drain coupled to respective drains of the fourth and fifth p-type transistors, a gate coupled to an output and the respective drains of the fourth and fifth transistors, and a source; and,

a fourth n-type transistor having a drain coupled to respective sources of the second and third n-type transistors, a source coupled to ground and a gate coupled to the gate and the drain of the first n-type transistor.

11) A delay locked loop circuit, comprising:

a phase detector capable of generating a phase difference signal responsive to an input signal and a feedback signal;

a charge-pump, coupled to the phase detector, capable of generating a voltage responsive to the phase difference signal;

a voltage regulator, coupled to the charge pump, capable of providing a current responsive to the voltage, wherein the voltage regulator includes a bias-generating device capable of providing a bias current;

a voltage-controlled delay line, coupled to the voltage regulator, capable of providing the feedback signal responsive to the current; and,

an interconnect, coupled to the charge pump and the voltage regulator, capable of providing the bias current.

12) The delay locked loop circuit of claim 11, wherein the bias-generating device in the voltage regulator is a MOSFET device.

13) The delay locked loop circuit of claim 12, wherein the MOSFET device is a first p-type transistor having a drain coupled to the interconnect and a source coupled to a voltage source.

14) The delay locked loop circuit of claim 13, wherein the voltage regulator includes:

a second p-type transistor having a gate coupled to a gate of the first p-type transistor and a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the second transistor gate and a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the third transistor gate and a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the fourth transistor gate and a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, a source coupled to ground and a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain and the respective gates of the third and fourth p-type transistors, a gate coupled to an input, and a source;

a third n-type transistor having a drain coupled to respective drains of the fourth and fifth p-type transistors, a gate coupled to an output and the respective drains of the fourth and fifth transistors, and a source; and,

a fourth n-type transistor having a drain coupled to respective sources of the second and third n-type transistors, a source coupled to ground and a gate coupled to the gate and the drain of the first n-type transistor.

15) A circuit, comprising:

a first circuit capable of providing an output signal responsive to a comparison of an input signal and a feedback signal; and,

a second circuit, coupled to the first circuit, capable of providing a bias current to the first circuit responsive to the input signal.

16) The circuit of claim 15, wherein the first circuit includes a first circuit component that is biased responsive to the bias current.

17) The circuit of claim 15, wherein the first circuit component includes a loop resistor.

18) The circuit of claim 15, wherein the first circuit component includes a charge-pump.

19) The circuit of claim 15, wherein the second circuit includes a bias-generating MOSFET device.

20) The circuit of claim 19, wherein the MOSFET device is a p-type device.

21) The circuit of claim 15, wherein the first circuit is a PLL circuit.

22) The circuit of claim 15, wherein the first circuit is a DLL circuit.

23) The circuit of claim 15, wherein the first circuit includes a voltage-controlled oscillator having an input, and the second circuit is capable of generating the bias current proportional to input current provided to the voltage-controlled oscillator input.

24) A circuit, comprising:

a first p-type device having a gate, a drain capable of outputting a current proportional to an output current and a source coupled to a voltage source;

a second p-type transistor having a gate coupled to the gate of the first p-type transistor and a source coupled to the voltage source;

a third p-type transistor having a gate coupled to the gate of the second transistor and a source coupled to the voltage source;

a fourth p-type transistor having a gate coupled to the gate of the third transistor and a source coupled to the voltage source;

a fifth p-type transistor having a gate coupled to the gate of the fourth transistor and a source coupled to the voltage source;

a first n-type transistor having a drain coupled to a drain of the second p-type transistor, a source coupled to ground and a gate coupled to the drain of the second p-type transistor;

a second n-type transistor having a drain coupled to a drain of the third p-type transistor, a gate coupled to an input and respective gates of the third and fourth p-type transistors, and a source;

a third n-type transistor having a drain coupled to respective drains of the fourth and fifth p-type transistors , a gate coupled to an output and the respective drains of the fourth and fifth p-type transistors, and a source; and,

a fourth n-type transistor having a drain coupled to respective sources of the second and third n-type transistor , a source coupled to ground and a gate coupled to a gate of the first n-type transistor.

25) The circuit of claim 24, wherein the circuit is included in an operational amplifier capable of generating a buffered signal at the output responsive to a signal at the input.

26) A method, comprising:

obtaining a current from a circuit responsive to an input signal;

providing a bias current to a circuit component in the circuit responsive to the current; and,

biasing the circuit component responsive to the bias current.

27) The method of claim 26, wherein the circuit is a PLL.

28) The method of claim 26, wherein the circuit is a DLL.

29) The method of claim 26, wherein the input signal is a clock reference signal.

30) The method of claim 26, wherein the circuit component is a loop resistor.

31) The method of claim 26, wherein the circuit component is a charge-pump.

32) The method of claim 26, wherein the circuit component is a phase mixer.

33) The method of claim 26, wherein the circuit component is an amplifier.

34) The method of claim 26, wherein the circuit component is a clock buffer.

35) A method, comprising:

obtaining a current representing frequency from a voltage regulator in a phase locked loop circuit; and,

providing a bias current to a circuit component in the phase locked loop circuit responsive to the current.

36) A method, comprising:

obtaining a current representing delay from a voltage regulator in a delay locked loop circuit; and,

providing a bias current to a circuit component in the delay locked loop circuit responsive to the current.

37) A circuit, comprising:

a first circuit capable of providing an output signal responsive to a comparison of an input signal and the output signal, wherein the first circuit includes a circuit component; and,

means, coupled to the first circuit, for providing a bias current to the circuit component responsive to the input signal.